

8/11/80

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## INTERNAL LETTER

Date: August 11, 1980

No: SFR/80-3

TO: Gary Burrell  
Loc/Dept: MD-22FROM: Steve Russell  
Loc/Dept: MD-45

CC:

Phone: 2505

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Subject: Preliminary Design Concepts for a Low-Cost GPS Set

An overall system concept for the GPS set is shown in the Attachment on page 1. To the left of the dotted line are the functional elements unique to the GPS set concept. I will be referring to this as the PVT Sensor. To the right of the dotted line is the CDU and those functions associated with the specific navigation requirements. The key point to be made is that the GPS sensor is unique to the NAVSTAR GPS concept and its function is to provide position, velocity, and time as determined by the GPS system. Other concepts such as display, navigation, grid reference system, and display data base should be treated independently in any future program. With this separation it will be possible to treat the GPS sensor as just another element of an integrated NAV system and eliminate the (seemingly endless) discussion of issues not directly related to the design and development of the GPS-based PVT sensor.

The civil application can be quite well served with a design that removes many of the features of the military set. Page 2 contrasts the differences in the two basic requirements. The civil set is a C/A-code-only tracker with no ionospheric correction and no Anti-Jam requirements. This results in considerable hardware savings.

A functional block diagram of a baseline set design is shown on page 3. Its essential features are:

- 1) Two-Channel design
- 2) Separate processors for receiver control and Nav processing.

Further functional breakdown is shown in the foldout block diagram on page 4. At this point in the design, many functional design decisions have been fixed. These include:

1. Frequency Plan
2. Two channel design with a rapid sequencing code tracking channel and an acquisition and data demodulation channel.
3. Code Generator and VCO architecture
4. Frequency tracking design
5. Initial synchronization design
6. Analog/Digital interface
7. Signal Presence monitor

The next level of detail would be the circuit implementations of these functions.

Page 5 is a statistical description of sensor cost estimates. These are very crude and based upon all of the data I have been exposed to. The numbers are undefendable for the most part. I still believe they represent the best estimates that we have at the present.

Major hardware cost elements for the GPS sensor are listed on page 6. The pie chart is an attempt to illustrate the relative cost impact of each element. Cost reduction on the most costly elements will produce the largest savings. The memory cost will be the most significant factor.

The frequency standard design will be very key to the success of a low-cost GPS set. The standard represents both a cost risk and a technical risk. The associated trade-offs are listed on page 7. Additional preliminary analysis is required before a meaningful spec can be developed. The figure on page 8 shows preliminary cost vs stability for the frequency standard. Considerably more data will be needed to make the necessary trade-off choices.

The frequency plan has a minor influence on frequency standard design but it has a major impact on the cost and performance of the variable frequency oscillators used in the code and carrier loops. Page 9 illustrates a couple of alternatives for the carrier loop. The VCXO and Digital VFO performance features are listed on page 10. The digital design is presently favored because it is amenable to LSI. Circuit design examples for the two contrasting approaches are shown on page 11. Finally, the cost vs setability for a VCXO design is given on page 12. Notice that the design range overlaps the TCXO/ovenized region.

Some examples of possible LSI partitioning for the code circuits and carrier VFO are shown on pages 13 and 14. The baseline design has been chosen to permit a high degree of LSI.

Preliminary size and power estimates are given on page 15. This will need considerable revision in the areas of Nav Processor and Power System but the other areas are still good estimates. I feel we can get to about 15 watts with a low-cost set but my hopes for smaller size are not great.

Last but not least are the major cost and technical risk areas identified on page 16. Attention to these areas very early in the program will minimize future problems.

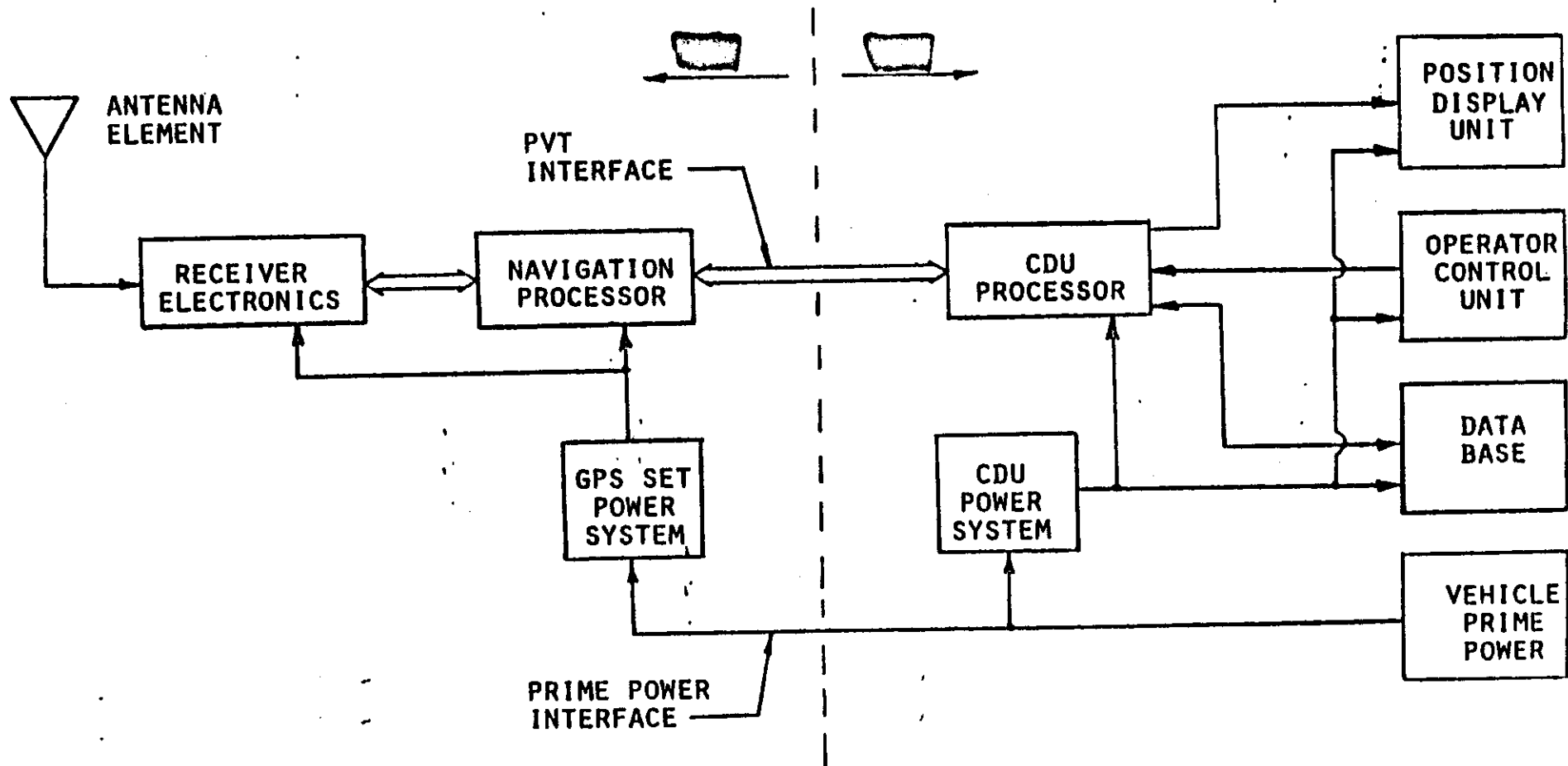
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Page 3

I have intended this to be a very brief look at some selected topics for the low-cost design. We will continue to improve our understanding and documentation of a low-cost set design.

SFR:csf

*Steve G. Russell*

## SYSTEM CONCEPT



## BASELINE DESIGN CONSIDERATIONS

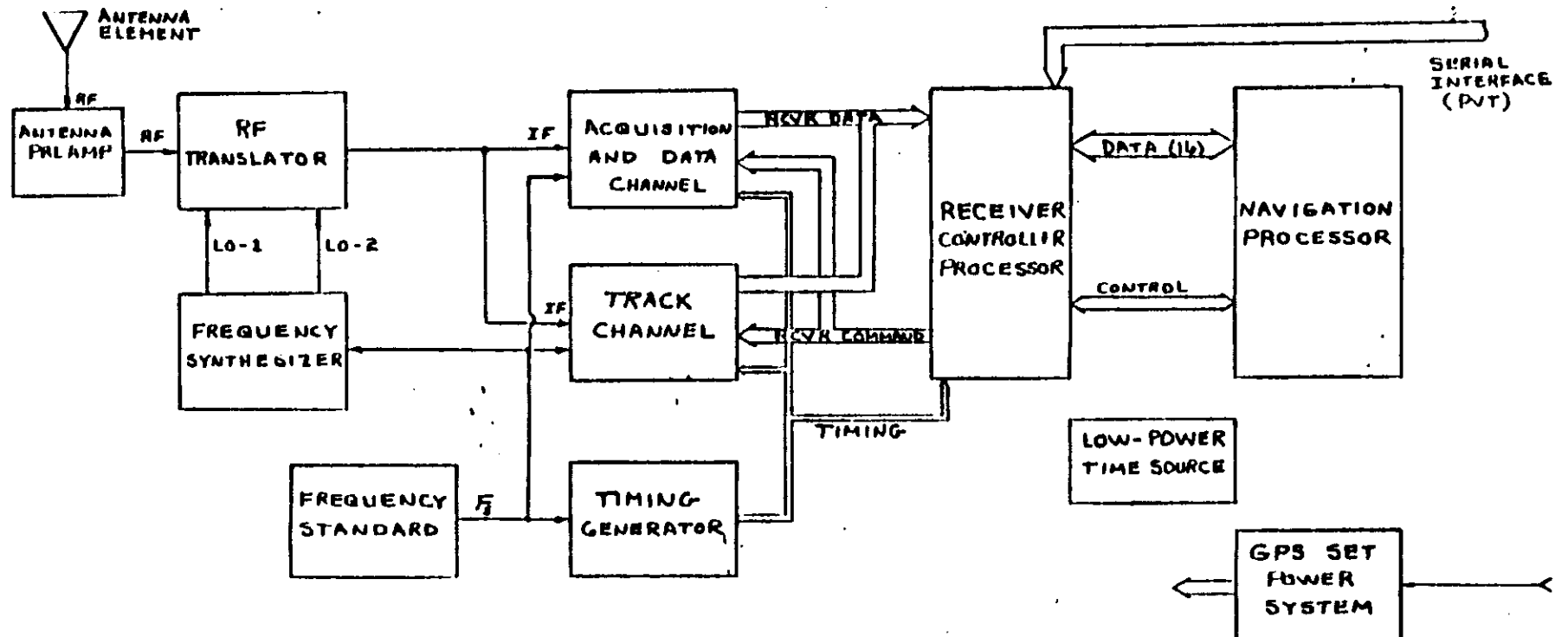
### MILITARY

- L1 AND L2
  - L1-L2 4x2 SWITCH
  - IONOSPHERIC CORRECTION
  - 10 MHZ CODE GEN
- C/A AND P CODES
  - COMPLEX HARDWARE SLEW CIRCUITS
  - WIDEBAND IF
- HIGH ANTI-JAM
  - PROMPT CHANNEL
  - DELAY-LOCK TRACKING
  - T-CODE PREVENTS JAMMER FEEDTHRU
  - 2 CODE MULTIPLIERS
  - FAST AGC
- HIGH ACCURACY
  - CARRIER PHASE TRACK
  - SLOW SEQUENCE
- HIGH STABILITY FREQ STD
- RADIATION HARDENING

### CIVIL

- L1 ONLY
  - NO SWITCH
  - NO CORRECTION
  - 1 MHZ CODE GEN
- C/A ONLY
  - NO SLEWING
  - NARROWBAND IF
- NO HOSTILE JAMMING
  - NO PROMPT CHANNEL
  - TAU-DITHER TRACKING
  - NO T-CODE
  - ONE CODE MULTIPLIER
  - NO PULSE JAMMING
- MODERATE ACCURACY
  - CARRIER FREQUENCY TRACK
  - FAST SEQUENCE
- MIN DESIGN FREQ STD
- NO RADIATION HARDENING

## BASELINE FUNCTIONAL BLOCK DIAGRAM



PRESENT  
CONFIDENCE  
LEVEL

CONFIDENCE  
GOAL

GPS SENSOR  
COST

99%

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\$12K

95%

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5K

80%

99%

3K

50%

95%

2K

30%

80%

1K

5%

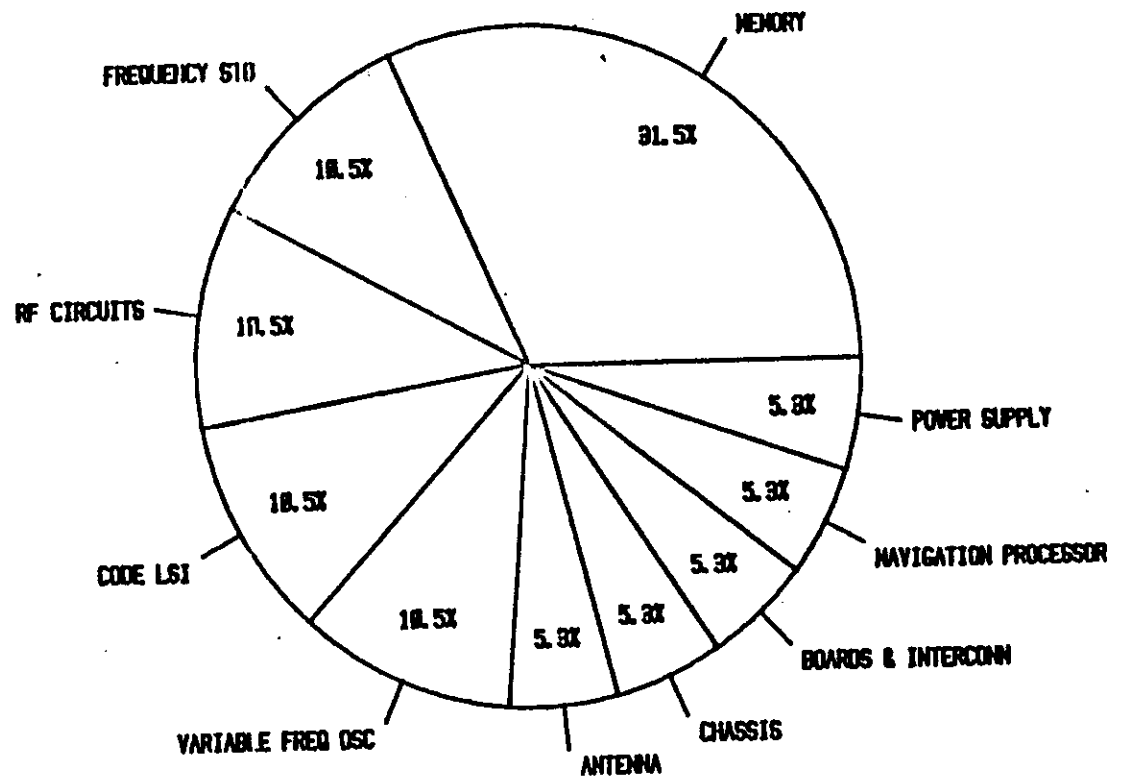
50%

.5K

MOST PROBABLE  
COST RANGE  
\$1K - 3K

## MAJOR HARDWARE COST ELEMENTS

- FREQUENCY STANDARD
- VARIABLE FREQUENCY OSC
- CODE LSI
- RF CIRCUITS
- POWER SUPPLY
- NAVIGATION PROCESSOR
- MEMORY
- BOARDS & INTERCONNECT
- CHASSIS
- ANTENNA

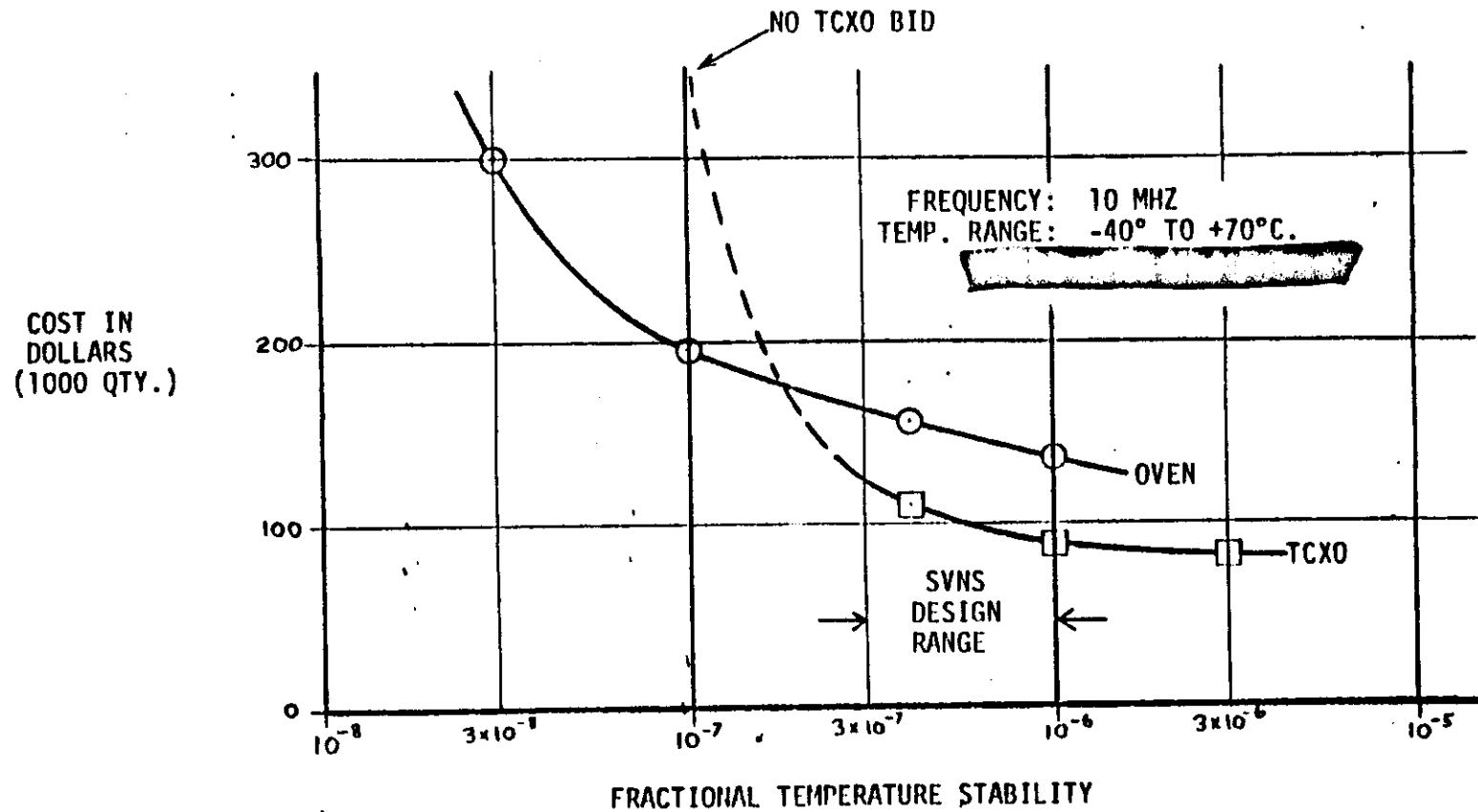


## FREQUENCY STANDARD TRADE-OFFS

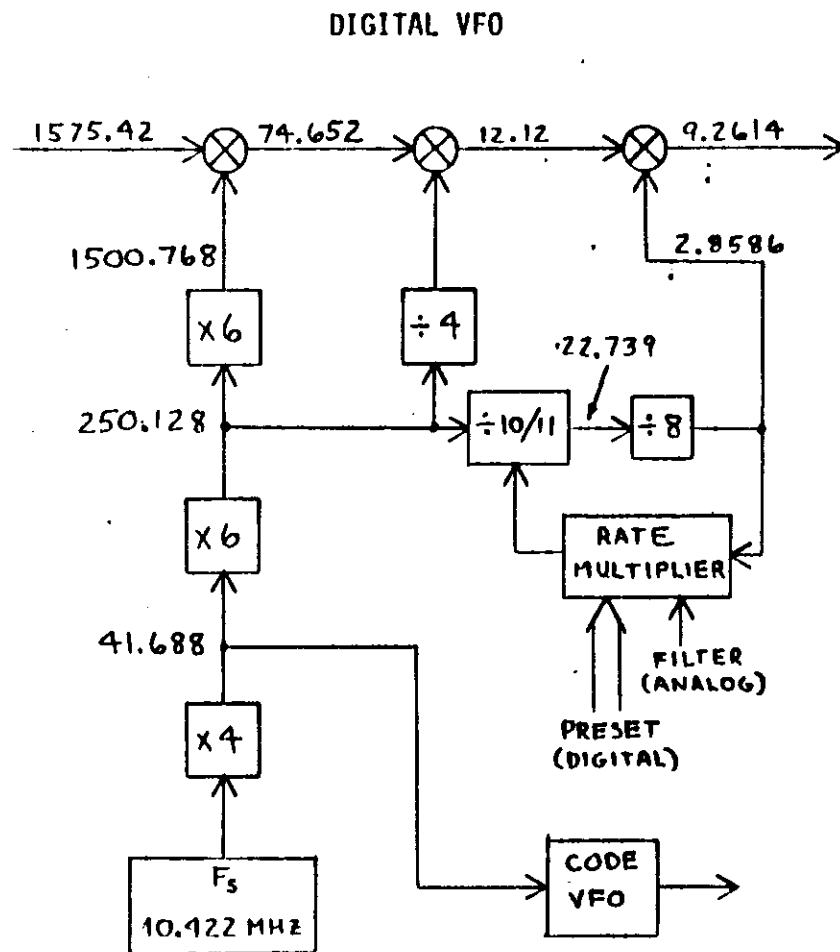
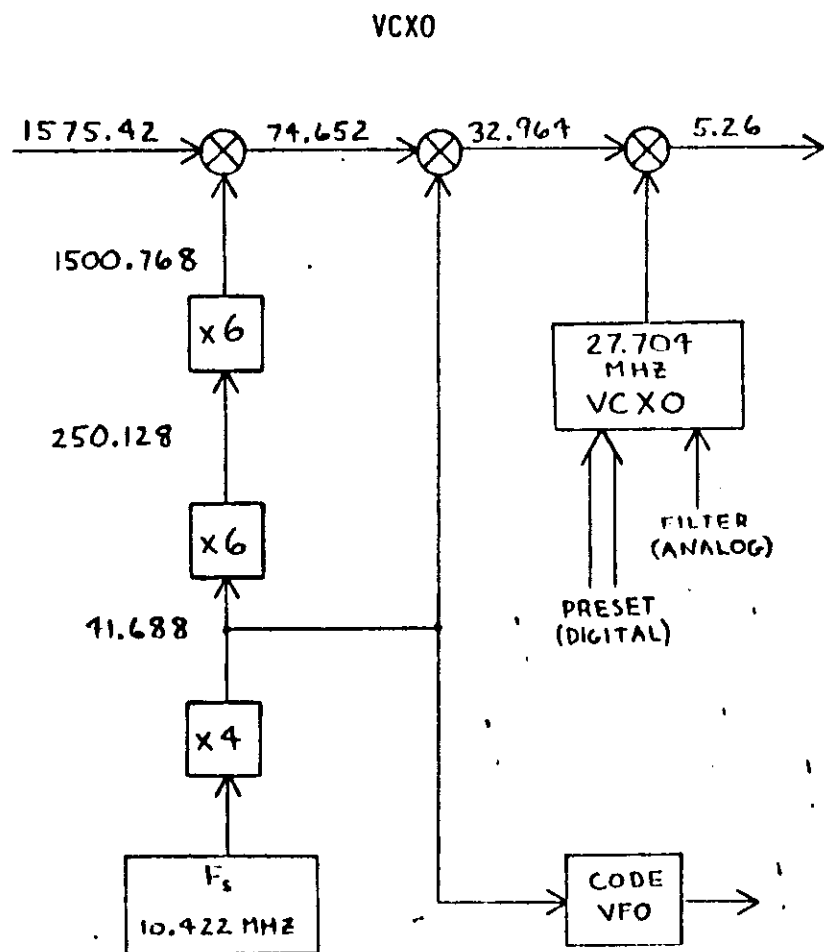
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- LARGE FREQUENCY VARIATIONS WITH TEMPERATURE CAUSE LONG ACQUISITION TIMES.
- TEMPERATURE STABILITY IS DRIVING FACTOR IN COST.
- OVENIZED OSCILLATOR REQUIRES HIGH POWER (3-6W) AND LONG WARM-UP TIME (5-10 MIN.).
- TCXO REQUIRES LITTLE POWER (200 MW) AND HAS QUICK WARM-UP (10 SEC.).
- CAN SUFFICIENT STABILITY BE OBTAINED AT LOW COST?
- CAN TCXO BE USED?

# FREQUENCY STANDARD COST VS. STABILITY



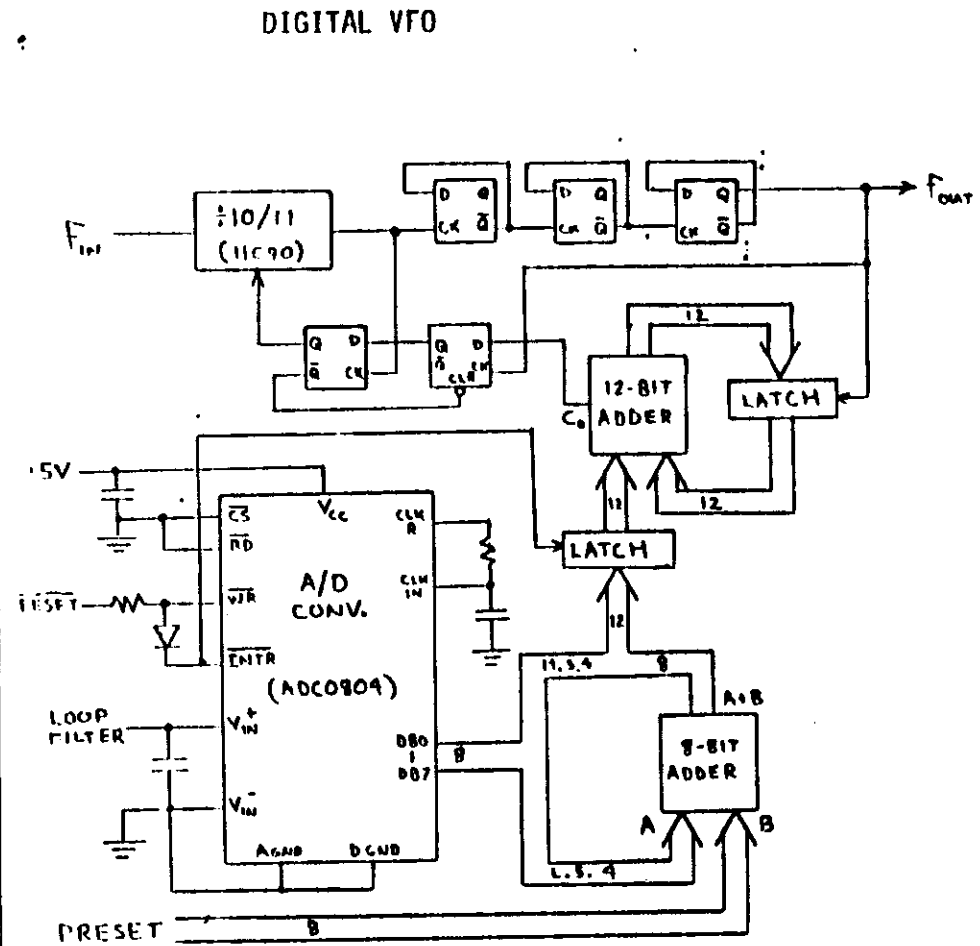
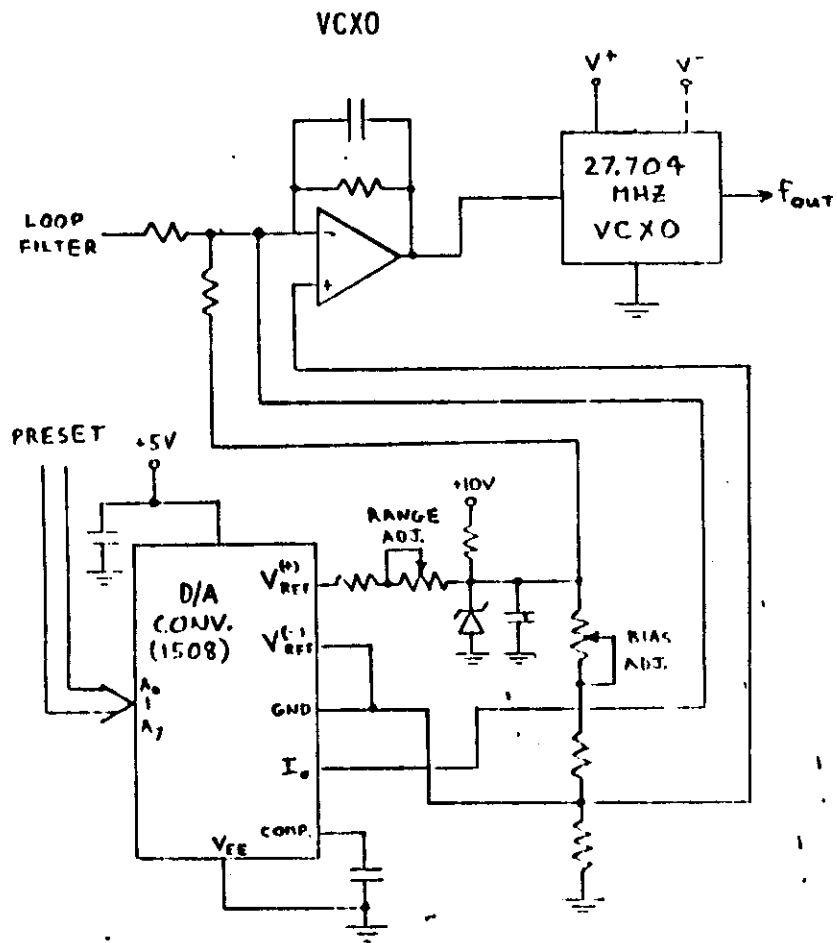
# • FREQUENCY PLAN ALTERNATIVES



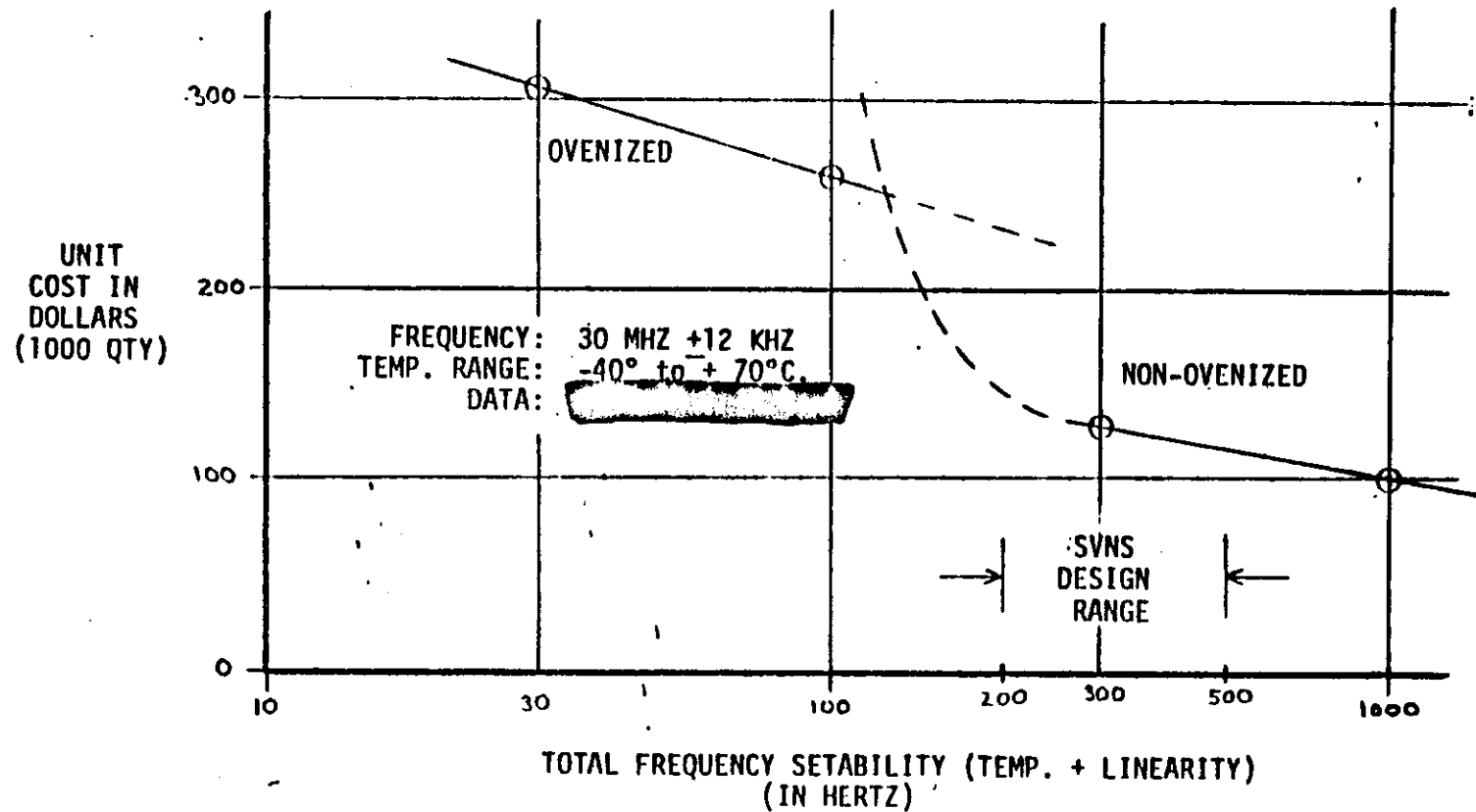
# VCXO AND DIGITAL VFO PERFORMANCE CONTRASTS

	VCXO	DIGITAL VFO
LINEARITY	DIFFICULT TO OBTAIN	ANALYTICALLY PREDICTABLE NON-LINEARITY
STABILITY	DIFFICULT TO OBTAIN	DETERMINED SOLELY BY REFERENCE
DIGITAL PRESET	REQUIRES HIGH-ACCURACY D/A	DIRECT
ANALOG FILTER INPUT	DIRECT	REQUIRES LOW-ACCURACY A/D
SUPPLY VOLTAGE(S)	MAY REQUIRE + AND - VOLTAGE, OR + VOLTAGE GREATER THAN 10V	SINGLE +5V SUPPLY
POWER	LOW - APPR. 100 MW.	HIGH - .5 TO 1 WATT
OUTPUT FREQUENCY	CONTINUOUSLY VARIABLE	DISCRETE
SPECTRAL PURITY	SPURIOUS-FREE	MANY SPURIOUS OUTPUTS
CUSTOM LSI	NOT APPLICABLE	YES

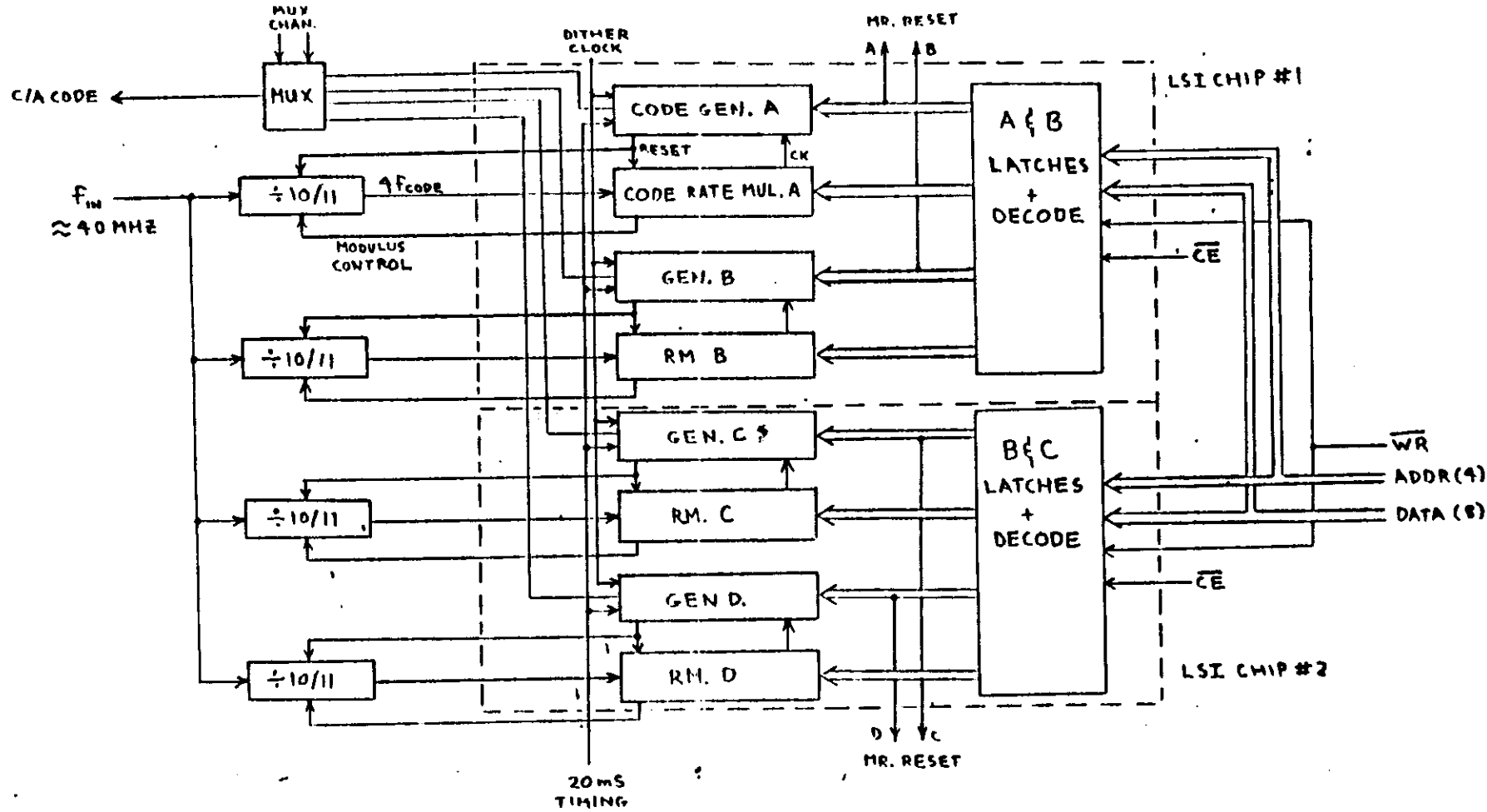
# DIGITAL VFO VS. VCXO CIRCUITRY



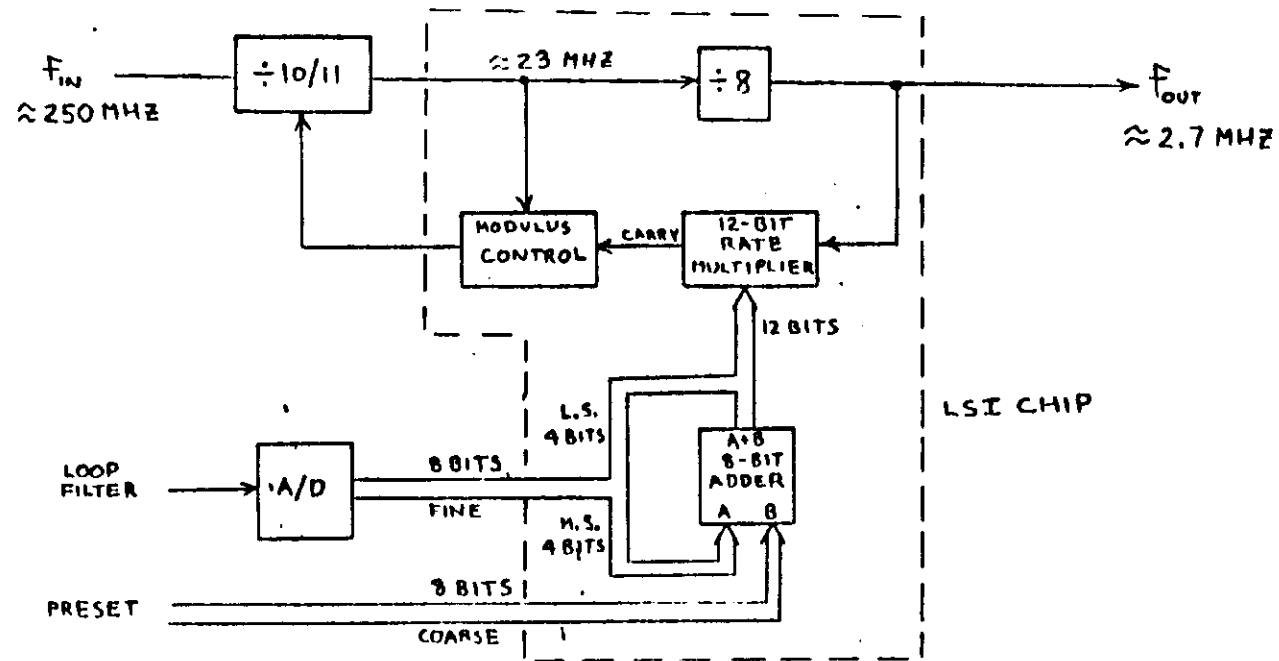
# VCXO COST VS. SETABILITY



# CODE LSI PARTITIONING



• DIGITAL CARRIER VFO LSI



# PRELIMINARY SIZE AND POWER ESTIMATES

	<u>FUNCTION</u>	<u>BOARD AREA</u>	<u>POWER</u>
1.	RF PREAMP	6	0.2
2.	SYNTHESIZER	9	0.5
3.	FREQ STD*	4	0.2
4.	RF TRANSLATOR	5	0.4
5.	DATA CHANNEL	30	3.0
6.	TRACK CHANNEL	30	3.0
7.	RCVR CONTROLLER	6	2.1
8.	NAV PROCESSOR	40	11.6
9.	LOW-POWER TIME SOURCE	2	-
10.	POWER SYSTEM**	15	10.5
		<u>147 IN<sup>2</sup></u>	<u>31.5 WATTS</u>

\* TCXO, 2" x 2" x 1"

\*\* 50% EFF, 3" x 5" x 1"

## RISK AREAS

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- MEMORY COST
- CUSTOM LSI COST & PERFORMANCE
- FREQUENCY STANDARD STABILITY
- MP THRUPUT
- ONE-BIT CODE POSITION DETECTOR
- ANTENNA COST